REMARKS

Claims 1 through 4, 6 through 9, and 15 through 24 are pending. The specification is not being amended.

Claims 1 through 4, and 6 through 9 are being amended. The amendments are being made in order to clarify the subject matter recited in these claims and for which protection is being sought. The claims are not being amended for patentability purposes, and no new matter is being added.

Claims 5, and 10 - 14 are being cancelled.

Claims 15 through 24 are new in order to remove multiple dependencies of amended Claims 4 and 6 - 8 currently on file. Again, no new matter is being added.

Responsive to the Examiner's request in section 5 of the Office Action, Applicants now affirm the election of Claims 1 through 4 and 6 - 10 provisionally made by Daniel D. Hill during a telephone conversion with the Examiner on March 2, 2006.

The drawings are currently rejected under 37 CFR 1.83(a) as not showing the calibration structure, the probing structure, and the optical alignment means. Applicant respectfully disagrees with the objection raised in the Office Action for the following reasons.

Referring to FIG. 1, page 6, line 8 and page 11, lines 14 - 22 explain that the element labelled 70 uses the element label 38 as the calibration structure. The probing structure recited in the claims is also shown in FIG. 1 and is explained on page 6, lines 16 - 21. In particular, the sub-module structure 32 is used in conjunction with "Laser Voltage Probing 40" and serves as the probing structure. Lastly, an example of the optical alignment means is shown in FIG. 11 and explained on page 11, lines 4 - 12.

It is therefore submitted that the calibration structure, the probing structure, and the optical alignment means are shown in the drawings.

In section 8 of the Office Action, Claims 6 - 8 are currently rejected on the grounds that the calibration structure, the probing structure, and the optical alignment means one not clearly identified in the drawings. However, as explained above in relation to section 7 of the Office Action, these features are shown in the drawings.

Claims 1 through 4, 9 and 10 are currently rejected under 35 USC § 102(b) as being anticipated by US 5,570,035 (Dukes et al.). Claim 10 has been cancelled. Applicants are traversing this rejection.

The application presently contains three independent claims, namely Claims 1, 2 and 3. Below, Applicants explain that the Dukes et al. document does not disclose all of the elements of Claims 1, 2 and 3.

According to col. 1, lines 17 - 25, Dukes et al. relates to a built-in self test circuitry for integrated circuits. In particular, Dukes et al. relates to an integrated circuit chip or a multi-chip module incorporating an internal built-in self test circuit for providing a visual feedback to a tester (a human being) through a packaging material that encapsulates the integrated circuit. Col. 2, lines 25 - 36 explains that the Built-In Self Test (BIST) circuitry comprises one or more digital micro-electronic circuits. A pair of leads connects the BIST to an electrically activated indicator device, such as a Light Emitting Diode (LED).

Clarified Claim 1 recites a test structure for performance evaluation and/or calibration of a failure analysis instrument. The structure has an analysis module including at least one submodule test structure that is arranged such that analysis of the at least one submodule test structure by the failure analysis instrument provides at least one physical parameter for use in testing of the failure analysis instrument. Analogous recitations can be found in clarified independent Claims 2 and 3.

The Dukes et al. document does not teach "a test structure for performance evaluation and/or calibration of a failure analysis instrument" as recited in Claim 1. The Dukes et al. document does not teach "an integrated circuit for performance evaluation and/or calibration of a failure analysis instrument" as recited in Claim 2. Also, the Dukes et al. document does not teach "a system for performance evaluation and/or calibration of a failure analysis instrument" as recited in Claim 3. As mentioned above, the circuitry of the Dukes et al. document is a self-test circuit that activates an LED when a failure has occurred. Hence, it

can be seen that the circuitry as described in Dukes et al. cannot be used to test a failure analysis instrument, rather Dukes et al. effectively discloses a very crude failure analysis tool integrally formed with an actual integrated circuit to be tested. Consequently, Dukes et al. does not relate to performance evaluation and/or calibration of a failure analysis instrument.

In view of the reasoning provided above, Applicants submit that the Dukes et al. document does not anticipate Claims 1, 2 or 3.

Claims 4 and 6 through 9 depend from Claim 1. By virtue of this dependence, Claims 4 and 6 through 9 are also not anticipated.

Claims 15, 17, 19, 21 and 23 depend from Claim 2. By virtue of this dependence, Claims 15, 17, 19, 21 and 23 are also not anticipated.

Claims 16, 18, 20, 22 and 24 depend from Claim 3. By virtue of this dependence, Claims 16, 18, 20, 22 and 24 are also not anticipated.

The case is believed to be in condition for allowance and notice to such effect is respectfully requested. If there is any issue that may be resolved, the Examiner is respectfully requested to telephone David G. Dolezal.

Respectfully submitted,

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